FPGA to C6x Interface

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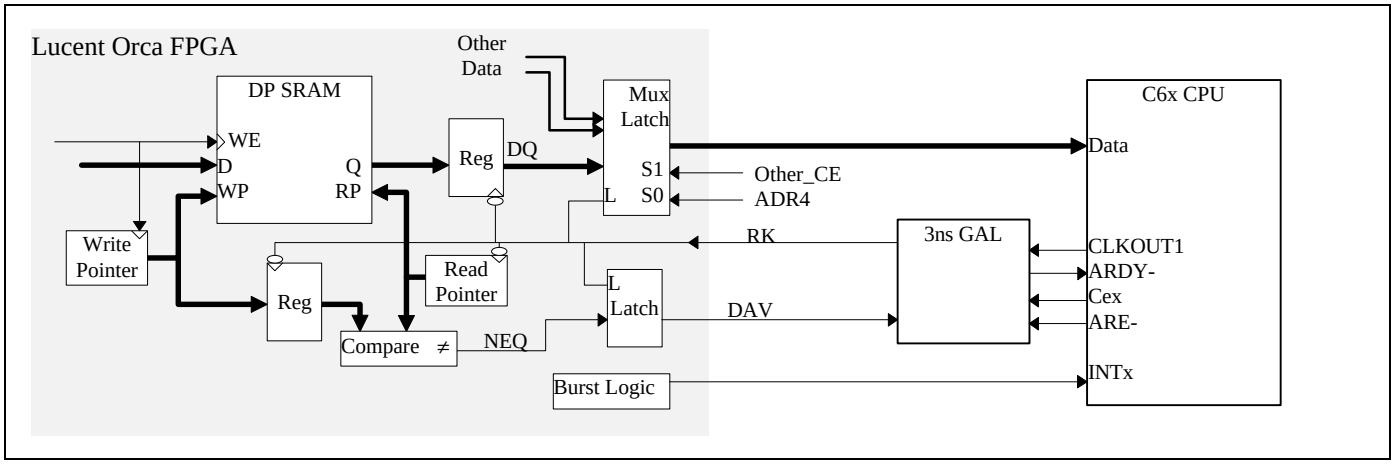
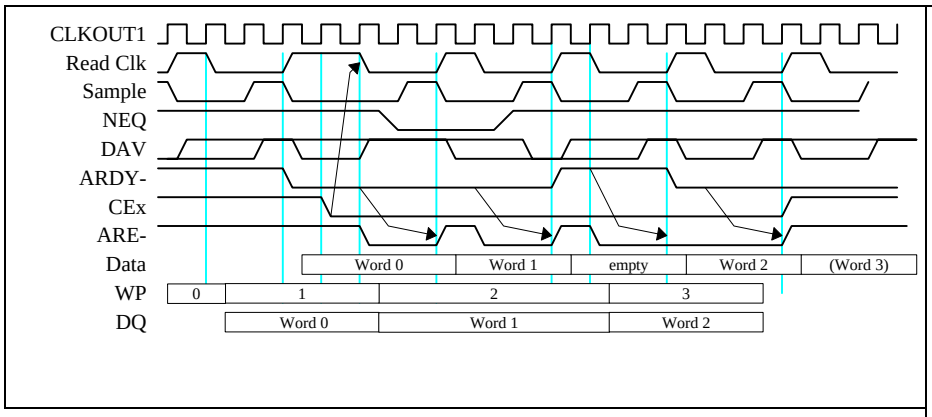
This describes how to do high speed transfers from an FPGA to the C6x. This circuit uses a high speed GAL to synchronize signals from the 200MHz C6x to the slower FPGA. The FPGA includes an internal 16-word FIFO with a burst counter that allows data to be transferred in bursts using the C6x on chip DMA controllers.





PAL Pins:

Clkout1	200MHz clock from C6x
/CEx	Chip enable to read FPGA FIFO
/Other_CE	Chip enable to read other data
/ARE	Asynchronous Read Enable
/AWE	Asynchronous Write Enable
/ARDY	Ready input to C6x
DAV	Data available in FPGA FIFO
RK	Read clock to FPGA
SAMPLE	Internal Timing pulse
VALID	Internal flag to control ARDY

PAL equations:

```
SAMPLE  := /SAMPLE*/RK;        ! Allow RD_CLOCK

RK := SAMPLE                   ! Cycle normally till DAV
+ RK*VALID*/CEx                ! Hold if DAV till C6x reads a word
+ RK*OTHER_CE                  ! Hold if other data sources being read

VALID := SAMPLE*DAV            ! Sample DAV
+ /SAMPLE*VALID                ! Hold

ARDY := SAMPLE*DAV ! Same as VALID
+ /SAMPLE*VALID
+ RK*(ARE+AWE)                 ! but assert if other read or write
```

Notes:

This circuit has not been tested or simulated. It's based on estimated timings for C6x chip of 2ns Tco and 2ns setup. Actual timings have not been released yet. Also note that the C6x peripherals document (page 6-36) claims that ARDY timing can't be used with ARE strobes of less than 3 cycles. I think it can, but TI doesn't seem to be able to answer this question.

Timings for the data path are very tight. The Tco time for the FPGA must be kept to 10ns which requires minimal loading on the data pins, and optimized FPGA placement and routing for the RK pin and data pins. This will probably not work if other devices share the C6x data bus. If other devices need access to the C6x, they should go through the FPGA.

References:

Lattice GAL data sheet
Lucent Orca 2Txxa data sheet